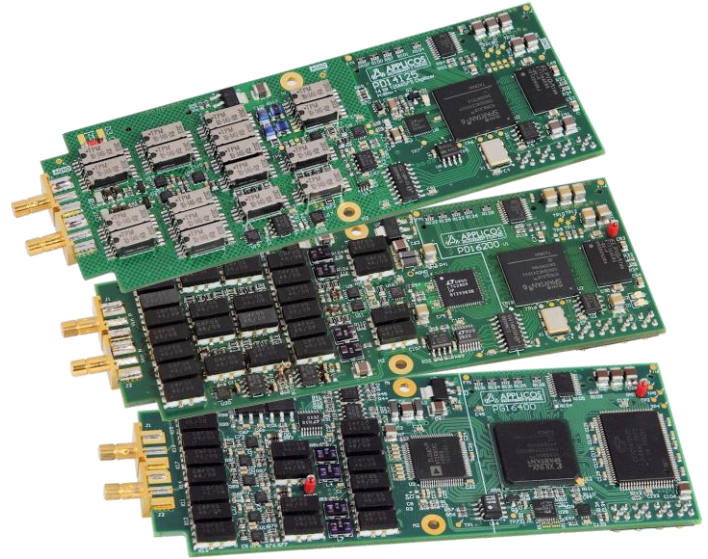


PA72 Series - PXI Generator & Digitizer platform



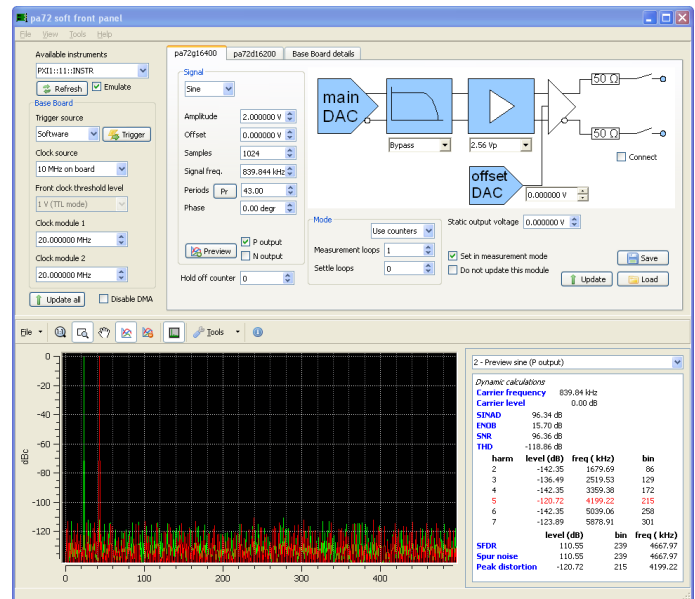
Features

- Flexible analog signal generation and capture platform
- Two daughter board slots
- On-board high performance clock source
- On-board high accuracy voltmeter
- Hybrid slot compatible
- 1ppm clock stability / 0.5ps clock jitter

The PA72 is a PXI base board designed to carry one or two high performance analog daughter boards. The base board contains all common hardware like; clock source, trigger circuitry, bus interface, supply regulation and a high precision voltmeter. The daughter boards determine the actual analog performance. The PA72 concept provides a flexible and cost effective solution for medium and high end analog functions.

The two daughter board slots can contain one of the available Generator or Digitizer boards listed on page 3. Also custom daughter boards can easily be created.

The PA72 uses the 32-bit PXI bus and supports burst mode. This allows up to 132MByte data throughput. The J2 con-connector is a small version to make it hybrid slot compatible.



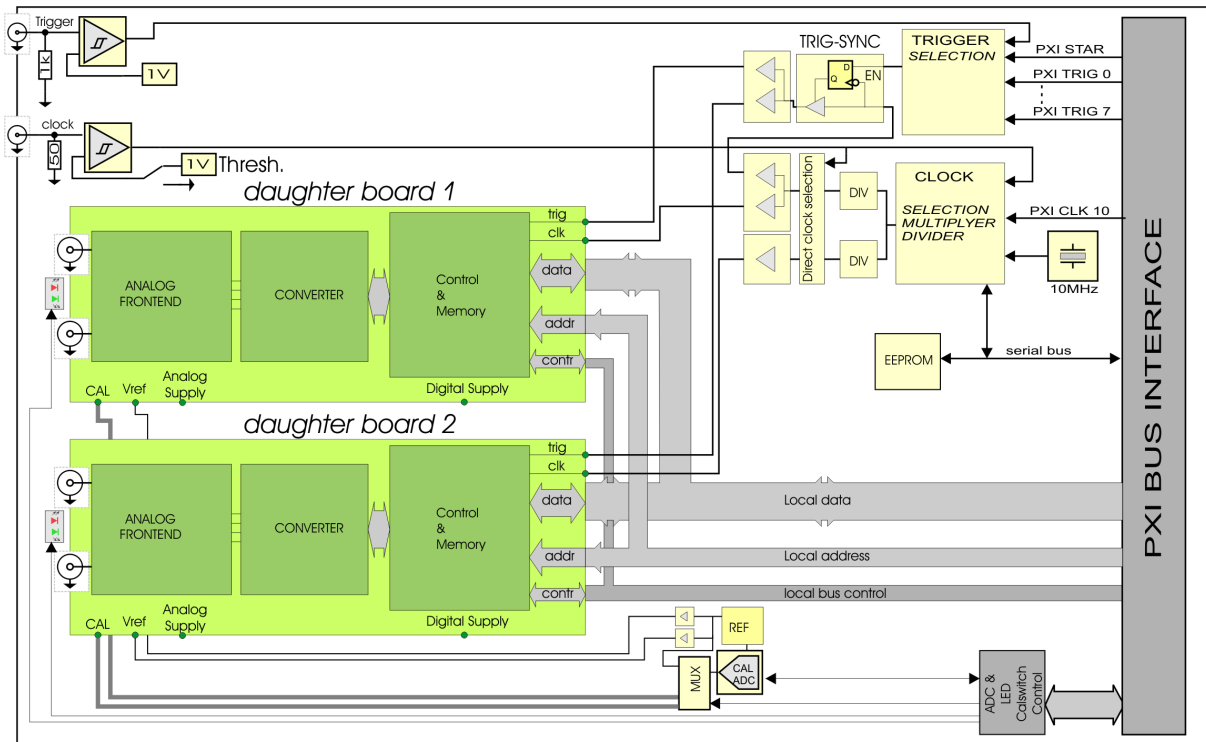
User control panel for the PA72 and an AWG daughter board

The PLL clock source is capable of generating any frequency between 2kHz up to 945MHz. This allows a wide range of daughter boards to be supported. The frequency stability is better than 1ppm and the jitter only 0.5ps. The frequency can be locked to the PXI backplane 10MHz or an external clock.

The on-board high accuracy voltmeter is used for automatic calibration. Most daughter boards also support measuring external DC voltages.

PA72 Series - PXI Generator & Digitizer platform

Block Diagram



Description:

The PA72 base board contains a clock generator, trigger circuitry, a digital voltmeter and the PXI bus interface. In the above diagram the base board functions are yellow and the daughter board functions are green.

The clock generator is a low jitter PLL clock that has less than 0.5ps jitter for low loop filter bandwidths. With higher loop filter bandwidths, frequency settling time can be less than 250ms.

The main clock frequency ranges from 2kHz up to 945MHz with a resolution of less than 1 kHz. Each daughter board

slot has its own divider. Therefore the clock for each daughter board can be different while maintaining proper synchronization. The PLL clock generator features a high stability low noise and low jitter 10MHz on-board reference clock with 1ppm frequency stability. In addition the PLL can be locked to the PXI backplane clock or to an external reference clock. Also can the on-board clock source be bypassed by an external clock.

The trigger input supports edge and level triggering and positive and negative going trigger signals. The trigger source can be software, PXI-Star, PXI 0-7 or external.

Specifications PA72 base board:

PLL clock

Frequency range 2kHz to 945MHz
 Sync possibilities 10MHz backplane or 10MHz external clock
 PLL lock time 250ms - 1s (depending on loop filter BW)
 Jitter 0.5ps typical

External clock input

Clock rate DC to 500MHz
 Treshold level 0V or 1V (programmable)
 Input impedance 50-Ohm

Trigger input

Threshold level 1V
 Input impedance 1k Ohm
 Max input level -0.5V to +5.5V
 Coupling DC

Trigger sources

External, PXI STAR, PXI TRIG 0..7, Software trigger
 Each trigger can be programmed to be edge or level and positive or negative going. Independent trigger source selection per channel

PA72 Series - PXI Generator & Digitizer platform

Brief specifications of available daughter boards

PA72G16400, 16-bit / 400Msps AWG

Channels	1
Resolution	16-bit
Update rate with PA72 clock	2kHz to 400MHz
Update rate external clock	DC to 400MHz
Pattern depth	8M-words
Output ranges Single ended	0.32Vp to 2.56Vp in 6 ranges
Output ranges Differential	0.64Vp to 5.12Vp in 6 ranges
Output offset voltage	-2.56 to +2.56V (>14-bit resolution)
Output configuration	50-Ohm, Single Ended or Differential
Output filters	Bypass, 60MHz, 30MHz
Absolute accuracy (V_{out+})	$\pm(250\mu V + 0.1\%$ of range +0.1% of value)
Relative accuracy	$\pm 0.006\%$
SNR (200Msps, 5Vpp diff.)	69dB @ f-out = 1MHz (BW: 0-80MHz)
SNR (200Msps, 5Vpp diff.)	67dB @ f-out = 10MHz, (BW: 0-80MHz)
THD (200Msps, 2.5Vpp diff.)	84dB @ f-out = 1MHz
THD (200Msps, 2.5Vpp diff.)	73dB @ f-out = 10MHz
SFDR (200Msps, 2.5Vpp diff.)	82dB @ f-out = 1MHz

PA72G14180, 14-bit / 180Msps AWG

Channels	1
Resolution	14-bit
Update rate with PA72 clock	2kHz to 180MHz
Update rate with ext. clock	DC to 180MHz
Pattern depth	64M-words
Output configuration	50-Ohm, Single ended or Differential
Output ranges	0.2Vp to 3.28Vp proportional ranging
Output filters	Bypass, 30MHz, 15MHz
DC-offset voltage	-2.56V to +2.56V
Absolute accuracy	$\pm(250\mu V + 0.1\%$ of range +0.1% of value)
Relative accuracy (INL)	$\pm 0.025\%$ of range
SNR (180Msps, 3.2Vpp diff.)	68dB @ f-out = 1MHz (BW: 0-70MHz)
SNR (180Msps, 3.2Vpp diff.)	64dB @ f-out = 10MHz, (BW: 0-70MHz)
THD (180Msps, 2.0Vpp diff.)	81dB @ f-out = 1MHz
THD (180Msps, 2.0Vpp diff.)	70dB @ f-out = 10MHz
SFDR (180Msps, 2.0Vpp diff.)	82dB @ f-out = 1MHz

PA72D16180, 16-bit / 180Msps Digitizer

Channels	1
Resolution	16-bit
Sample rate (PA72 and ext.)	1MHz to 180MHz
Memory depth	64M-words
Input ranges	0.256Vp to 3.072Vp in 8 ranges
Input configurations	50-Ohm, AC or DC, Diff. or Single Ended
DC-offset voltage	\pm the input range (16-bit resolution)
Input bandwidth	80MHz (typical)
Input filters	Bypass, 60MHz, 30MHz
Absolute accuracy (V_{out+})	$\pm(250\mu V + 0.1\%$ of range +0.2% of value)
Relative accuracy	$\pm 0.006\%$
SNR (180Msps, 4Vpp diff)	69dB @ f-in = 1MHz (BW: 0-80MHz)
SNR (180Msps, 4Vpp diff)	67dB @ f-in = 10MHz (BW: 0-80MHz)
THD (180Msps, 4Vpp diff)	85dB @ f-in = 1MHz
THD (180Msps, 4Vpp diff)	81dB @ f-in = 10MHz
SFDR (180Msps, 4Vpp diff)	83dB @ f-in = 1MHz

PA72D14130, 14-bit / 130Msps Digitizer

Channels	1
Resolution	14-bit
Sample rate (PA72 and ext.)	1MHz - 130MHz
Memory depth	64M-word
Input configuration	Differential or single ended
Input ranges (span)	0.338Vp to 3.6Vp in 8 ranges
DC-offset voltage	-3.6V to +3.6V
Input operating area	-3.6V to +3.6V
Input impedance	10kOhm or 50-Ohm, DC or AC
Input filters	Bypass, 30MHz, 15MHz
Absolute accuracy	$\pm(250\mu V + 0.05\%$ of range +0.1% of value)
Relative accuracy (INL)	$\pm 0.025\%$ of range
SNR (130Msps, 3.2Vpp diff.)	66dB @ f-in = 1MHz (BW: 0-60MHz)
SNR (130Msps, 3.2Vpp diff.)	64dB @ f-in = 10MHz, (BW: 0-60MHz)
THD (130Msps, 3.2Vpp diff.)	78dB @ f-in = 1MHz
THD (130Msps, 3.2Vpp diff.)	74dB @ f-in = 10MHz
SFDR (130Msps, 3.2Vpp diff.)	80dB @ f-in = 1MHz

Module numbering:

The configuration of a PA72 module is determined as follows:

PA72-nm

n = daughter board 1 (top position)

m = daughter board 2 (bottom position)

Daughter board codes:

0 = empty
1 = PA72G16400
2 = PA72G14180
5 = PA72D16180
6 = PA72D14130

For example a PA72-15 is a PA72 base board with a 16-bit / 400Msps AWG in the top position and a 16-bit / 180Msps Digitizer in the bottom position